ABSTRACT OF THE DISCLOSURE

A test device and method for detecting alignment of active areas and memory cell structures in DRAM devices with vertical transistors. In the test device, parallel first and second memory cell structures disposed in the scribe line region, each has a deep trench capacitor and a transistor structure. An active area is disposed between the first and second memory cell structures. The active area overlaps the first and second memory cell structures by a predetermined width. First and second conductive pads are disposed on both ends of the first memory cell structures respectively, and third and fourth conductive pads are disposed on both ends of the first memory cell structures respectively.